

ABSTRACT OF THE DISCLOSURE

A shift left with carry instruction minimizes the number of instructions required for implementing a binary search. A multi-thread packet processor transfers a data packet from a flexible data input buffer to a packet task manager, dispatches the data packet from the packet task manager to a multi-threaded pipelined analysis machine, classifies the data packet in the analysis machine, modifies and forwards the data packet in a packet manipulator, wherein the analysis machine implements a binary search by executing a shift left with carry instruction to minimize the number of instructions required for the binary search. The multi-thread packet processor includes an analysis machine having multiple pipelines, wherein one pipeline is dedicated to directly manipulating individual data bits of a bit field, a packet task manager, a packet manipulator, a global access bus including a master request bus and a slave request bus separated from each other and pipelined, an external memory engine, and a hash engine.